SGS-THOMSON MICROELECTRONICS

# QN100 QUALITY NOTE

## MEMORY PRODUCTS QUALITY PROGRAM

The Corporate quality program of SGS-THOMSON is published as the SURE (Semiconductor Users Reliability Evaluation) Program. The quality program for memory products follows closely this Program. Described here are the particular controls that apply specifically to memories starting with the Lot Acceptance and AOQ assessment and followed by the program for memory product qualification, an indication of the the manufacturing SPC (Statistical Process Controls) and the Short and Long term reliability tests. On request, extra tests may be agreed with the customer at product qualification.

### Lot Acceptance

The role of a final Lot Acceptance sampling has changed from that of lot acceptance - although this still applies - more to the collection of statistical data about the outgoing quality, and the monitoring of the quality to the target defectivity in Parts Per Milion (ppm).

The Average Outgoing Quality (AOQ) is estimated from the results of Lot Acceptance testing. The measure developed by and used by SGS-THOMSON for the AOQ is known as the Average Outgoing Quality Estimator and is given by:

$$\frac{\text{Total Defective units in sample, with } d \leq c + 1}{\text{Total inspected units in samples of accepted lots}}$$

where d = number of defects in sample, c = acceptance number. The totals are those of ALL lots inspected (1st, 2nd, etc controls).

This AOQE converges towards the real AOQ as the number of sampled lots increases, even though an acceptance number of zero is used.

**Table 1. Finished Product Acceptance**

| Subgroup | Parameters | Minimum Sample Size | Acceptance Number |
|---|---|---|---|
| A1 | Visual and mechanical inspection | 315 | 0 |
| A2+A3+A4 | Cumulative electrical and inoperative mechanical failures | 315 | 0 |

**Table 2. Qualification**

| | | |
|---|---|---|
| 1 | Wafer Fabrication Major Changes | Tests selected to control the parameters that are affected by the change, varying from the design or mask set to the fabrication plant. |
| 2 | Assembly Major Changes | Tests selected to control the parameters that are affected by the change, varying from package material changes to the assembly plant. |
| 3 | Product Qualification | Tests selected to control the parameters depending on the type of package and whether the die is new or already qualified. |

**Table 3. Product Qualification, Ceramic Packages - Package Related Tests**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Physical Dimensions | 2016 | Published Data |
| 2 | Bond Strength | 2011 | |
| 3 | Die Attach | 2019 or 2027 | |
| 4 | Fine Leak | 1014 | Test Condition A1 |
| | Gross Leak | 1014 | Test Condition C1 |
| 5 | Lid Torque | 2024 | |
| 6 | Internal Water Vapour | 1018 | 5000 ppm (max) |
| 7 | Solderability: | | |
| | – FDIP Package | 2003 | 245°C, 5sec, Precondition Steam, 1hr |
| | – JLCC, LCCC Packages | CECC 90,000 | 215°C, 3sec, Precondition Steam, 1hr |
| 8 | Resistance to Solvents | 2015 | 4 Solvent Solutions |
| 9 | Salt Atmosphere | 1009 | Test Condition A, 35°C, 24hrs |
| 10 | Lead Integrity | 2004 | Test Condition B2 |
| 11 | Resistance to Soldering Heat | | 260°C, 10sec |
| 12 | Thermal Shock | 1011 | –55 to 125°C, 15 cycles |
| | Temperature Cycling | 1010 | –65 to 150°C, 100 cycles |
| | Moisture Resistance | 1004 | –10 to 65°C, RH = 90% |
| | Fine Leak | 1014 | Test Condition A1 |
| | Gross Leak | 1014 | Test Condition C1 |
| 13 | Mechanical Shock | 2002 | Test Condition B |
| | Vibration Variable Frequency | 2007 | Test Condition A |
| | Constant Acceleration | 2001 | Teat Condition E |
| | Fine Leak | 1014 | Test Condition A1 |
| | Gross Leak | 1014 | Test Condition C1 |
| 14 | Temperature Cycling | 1010 | –65 to 150°C, 10 cycles |
| | Constant Acceleration | 2001 | Test Condition E |
| | Fine Leak | 1014 | Test Condition A1 |
| | Gross Leak | 1014 | Test Condition C1 |

**Table 4. Product Qualification, Plastic Packages - Package Related Tests**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Physical Dimansions<br>Coplanarity PLCC, PSOJ, TSOP & JLCC Packages | 2016 | Published Data<br>Published Data |
| 2 | Bond Strength | 2011 | |
| 3 | Die Attach | 2019 or 2027 | |
| 4 | Solderability:<br>– PSO, PSOJ, PLCC & TSOP Packages<br>– PDIP Package | CECC 90,000<br>2003 | 215°C, 3sec, Precondition Steam, 8hrs<br>245°C, 5sec, Precondition Steam, 8hrs |
| 5 | Resitance to Solvents | 2015 | 4 Solvent Solutions |
| 6 | Salt Atmosphere | 1009 | Test Condition A, 35°C, 24hrs |
| 7 | Lead Integrity | 2004 | Test Condition B2 |
| 8 | Resistance to Soldering Heat:<br>– PDIP Package | | 260°C, 10sec |
| 9 | Moisture-induced stress sensitivity for surface mount devices | JEDEC JESD22-A112 | |

**Table 5. Product Qualification, Ceramic Packages - Die Related Tests**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Operating Life Test | 1005 | 140°C, $V_{CC}$ = 6 to 7V, 500hrs |
| 2 | Retention Bake (EPROM) | 1008 | 250°C, 500hrs |
| 3 | Temperature Cycling | 1010 | –65 to 150°C, 1000 cycles |
| 4 | Thermal Shock | 1011 | –55 to 125°C, 500 cycles |
| 5 | Electrostatic Discharge | 3015 | 1500Ω, 100pF, 2000V (min) |
| 6 | Electrostatic Discharge | EIAJ IC-121 | 0Ω, 200pF, 200V (min) |
| 7 | Latch-up | JEDEC STD-17 | Current Injection 200mA (min), Overvoltage 14V (min) |

**Table 6. Product Qualification, Plastic Packages - Die Related Tests**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Operating Life Test [1] | 1005 | 140°C [2], $V_{CC}$ = 6 to 7V, 500hrs |
| 2 | Retention Bake (OTP, EEPROM) | 1008 | 150°C, 1000hrs |
| 3 | Write/Erase Cycling (EEPROM, FLASH) | | Published Data |
| 4 | Temperature, Humidity, Bias [1] | CECC 90,000 | 85°C, RH = 85%, $V_{CC}$ = 5V, 1000hrs |
| 5 | Temperature Cycling [1] | 1010 | –65 to 150°C, 1000 cycles |
| 6 | Thermal Shock [1] | 1011 | –55 to 125°C, 500 cycles |
| 7 | Pressure Pot [1] | | 121°C, 2Atm, 240hrs |
| 8 | HAST | CECC 90,000 | 130°C, RH = 85%, 96hrs |
| 9 | Electrostatic Discharge | 3015 | 1500Ω, 100pF, 2000V (min) |
| 10 | Electrostatic Discharge | EIAJ IC-121 | 0Ω, 200pF, 200V (min) |
| 11 | Latch-up | JEDEC STD-17 | Current Injection 200mA (min), Overvoltage 14V (min) |
| 12 | Soft Error Testing (SRAM) | | |

**Notes:** 1. Apply preconditioning flow on SMD devices before tests as per JESD22-A113.
2. 125°C for SRAM.

### Memory Product Qualification/Major Changes

Memory Product qualification is made on new memory products, new die designs and new packages and existing products when there are major changes to the design or manufacturing.

The tests performed depend on the parameters affected by a major change or the qualification of combinations of new die designs and new Plastic or Ceramic packages.

The tests performed are selected as appropriate from those listed in Tables 3 through 6.

### Statistical Process Control

One of the most powerfull tools implemented throughout the production of memory products is SPC. The final goal of the SPC program is to bring each critical step of the process to ”6 Sigma” capability ($Cp \geq 2$). Current controls are at Cp and Cpk  1.33. For example, in a typical wafer processing line more than 200 variables may be controlled for SPC. Data is gathered and analysed by on-line computers and provides up-to-the minute control charts (eg $\overline{X}$, R charts). The critical process steps are defined by FMEA (Failure Mode and Effects Analysis).

A selection of the most important SPC steps and the Cp and Cpk results is regularly available and can help customers to avoid the costly qualification of new products when the products come from a qualified design and a manufacturing process that is demonstrated to be under control.

The Table 7 and Table 8 show some typical SPC results from both wafer fabrication and assembly processes.

**Table 7. Statistical Process Control, Wafer Fabrication, CMOS EPROM (0.8 micron)**

| # | Parameter | Dependant Performance | CP | CPK |
|---|---|---|---|---|
| 1 | VTH Field Minimum P-Channel Transisitor | Latch-up Related | 2.53 | 2.56 |
| 2 | VTH Field Minimum N-Channel Transistor | Latch-up Related | 2.06 | 1.84 |
| 3 | Gate Oxide Thickness | Data Retention & ESD | 1.44 | 1.44 |
| 4 | Interpoly Oxide Thickness | Data Retention | 1.47 | 1.34 |
| 5 | Intermediate Dielectric Thickness | Data Retention | 1.91 | 1.83 |

**Table 8. Statistical Process Control, Ceramic Package Assembly EPROM**

| # | Parameter | Dependant Performance | CP | CPK |
|---|---|---|---|---|
| 1 | Shear Test | Die Attach | (*) | 3.25 |
| 2 | Bond Strength | Bond Weakness | (*) | 2.55 |
| 3 | SN Thickness | Thin Plating | 1.56 | 1.50 |
| 4 | Lead Lenght | Cropping | 4.47 | 3.37 |

**Note:** *. One side limit only.

## Short Term Reliability Testing

In order to provide a rapid feedback on product reliability to manufacturing, a series of Short Term Reliability tests are performed on a weekly basis. These are summarised in Table 9 and Table 10.

**Table 9. Short Term Reliability Tests, Ceramic Packages**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Thermal Shock | 1011 | –55 to 125°C, 60 cycles |
| 2 | Retention Bake (EPROM) | | 180°C, 72hrs |
| 3 | Solderability | 2003 | 245°C, 5sec, Precondition Steam, 1hr |
| 4 | Resistance to Solvents | 2015 | 4 Solvent Solutions |
| 5 | Physical Dimensions | 2016 | Published Data |
| 6 | Lead Integrity | 2004 | Test Condition B2 |
| 7 | Hermeticity: | 1014 | |
| | – Fine Leak | | Test Condition A1 |
| | – Gross Leak | | Test Condition C1 |
| 8 | Lead Torque | 2024 | |

**Table 10. Short Term Reliability Tests, Plastic Packages**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Temperature Cycling | 1010 | –65 to 150°C, 100 cycles |
| 2 | Write/Erase Cycles (EEPROM & FLASH) | | Published Data |
| 3 | Solderability: | | |
| | – PSO, PSOJ, PLCC & TSOP Packages | CECC 90,000 | 215°C, 3sec, Precondition Steam, 8hrs |
| | – PDIP Package | 2003 | 245°C, 5sec, Precondition Steam, 8hrs |
| 4 | Resistance to Solvents | 2015 | 4 Solvent Solutions |
| 5 | Physical Dimensions | 2016 | Published Data |
| 6 | Lead Integrity | 2004 | Test Condition B2 |
| 7 | Pressure Pot | | 121°C, 2Atm, 240hrs |

## Long Term Reliability Testing

Long Term Reliability tests are performed to provide evidence of the life time reliability of memory products. Sampling is made either monthly, 3 or 6 monthly depending on the tests performed. Table 11 and Table 12 summarise the tests.

**Table 11. Long Term Reliability Tests, Ceramic Packages**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Operating Life | 1005 | 140°C, $V_{CC}$ = 6V, 1000hrs |
| 2 | Retention Bake (EPROM) | 1008 | 250°C, 500hrs |
| 3 | Electrostatic Discharge | 3015 | 1500Ω, 100pF, 2000V (min) |
| 4 | Internal Water Vapour | 1018 | 5000 ppm (max) |
| 5 | Temperature Cycling | 1010 | –65 to 150 °C, 500 cycles |

**Table 12. Long Term Reliability Tests, Plastic Packages**

| Subgroup | Test Procedure | MIL-STD-883 Procedure | Test Conditions |
|---|---|---|---|
| 1 | Operating Life | 1005 | 140°C [1], $V_{CC}$ = 6V, 1000hrs |
| 2 | Retention Bake (OTP & EEPROM) | 1008 | 150°C, 1000hrs |
| 3 | Temperature, Humidity, Bias | CECC 90,000 | 85°C, RH = 85%, $V_{CC}$ = 5V, 1000hrs |
| 4 | Electrostatic Discharge | 3015 | 1500Ω, 100pF, 2000V (min) |
| 5 | HAST | CECC 90,000 | 130°C, RH = 85%, 96hrs |
| 6 | Temperature Cycling | 1010 | –65 to 150 °C, 500 cycles |

**Note:** 1. 125°C for SRAM.

## Conclusion

SGS-THOMSON believes that the extensive attention given to process control and product evaluation, combined with clear design rules and a well designed technology base, give the Company a world class overall quality rating.

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1996 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES
Australia - Brazil - Canada - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.